REMARKS

In the Office Action, the Examiner rejected Claims 1-14, which were all of the then pending claims, over the prior art, principally U.S. Patent 6,355,563 (Cha, et al.). Specifically, Claims 1, 2 and 9 were rejected under 35 U.S.C. 102 as being fully anticipated by Cha, et al; Claim 11 was rejected under 35 U.S.C. 103 as being unpatentable over Cha, et al; and Claims 3-8, 10 and 12-14 were rejected under 35 U.S.C. 103 as being unpatentable over Cha, et al. in view of U.S. Patent 6,753,538 (Musil, et al.).

Applicants are herein amending Claim 1 to better define the subject matter of the claim. New Claims 15 and 16, which are dependent from Claim 1, are being added to describe preferred features of the invention.

For the reasons discussed below, Claims 1-16 patentably distinguish over the prior art and are allowable. The Examiner is, thus, requested to reconsider and to withdraw the rejection of Claims 1, 2 and 9 under 35 U.S.C. 102 and the rejections of Claims 3-8 and 10-14 under 35 U.S.C. 103, and to allow Claims 1-16.

The present invention generally relates to high resolution cross-sectioning of polysilicon features using a dual beam tool. As discussed in the present application, it is very important to be able to obtain precise measurements and cross sections of critical polysilicon structures that are developed on a silicon wafer. Prior art processes that attempt to do this often result in severe rounding of the top edges of the polysilicon features.

The present invention addresses this problem, and in particular, provides a method for measuring these features without destruction or deformation of the features. Generally, this is done by encapsulating the polysilicon features of interest with a metal coating to preserve the profile of those features. Then, the polysilicon is etched from the encapsulating metal to remove the polysilicon while leaving the profile of the polysilicon surface features preserved in the encapsulating metal.

Cha, et al. discloses a semiconductor fabrication process in which a low-k dielectric material is integrated with copper metallization. Various steps are used in this process, including formation and removal of dummy vias 20. Also, in this process, a layer 22 is used initially to encapsulate the dummy vias 20, and then portions of the layer 22 are removed to expose the top surfaces of the dummy vias.

There is thus a very important general difference between the present invention and Cha, et al. Specifically, Cha, et al is related to integrating low dielectric constant materials in the manufacture of integrated circuits, while the present invention is directed to measuring polysilicon features.

This general difference is reflected in a number of more specific differences between Cha, et al. and the instant invention. One such specific difference is that, with the present invention, the polysilicon features of interest are encapsulated within the metal coating in order to preserve the profile of those polysilicon features, and then, when the polysilicon itself is removed, that profile is left preserved in the encapsulating metal. This, Cha, et al. does not do. Instead, with the procedure disclosed in cha, et al, portions of the encapsulating metal liner 22 are themselves removed, in order to allow removal of the dummy vias 20. As a result, the metal liner 22 does not preserve the profile of the dummy vias when those vias are removed.

Claim 1 is being amended to describe more expressly the above-discussed difference between this invention and the prior art. In particular, as amended herein, Claim 1 sets forth the steps of encapsulating the polysilicon features of interest with a metal coating to preserve the profile of the polysilicon features, and etching and cleaning the polysilicon from the encapsulating metal to remove the polysilicon while leaving the profile of the polysilicon surface features preserved in the encapsulating metal.

The other references of record have been reviewed, and these other references, whether considered individually or in combination, also do not disclose or suggest this feature of the present invention. In particular, Musil, et al. was cited for its disclosure of the use of a scanning electron microscope to image and evaluate preserved polysilicon features. This reference, though, does not teach preserving the polysilicon profile in the manner described in Claim 1. Musil, et al. also does not teach measuring such a preserved profile.

The above-discussed feature of the present invention is of utility because, among other reasons, it helps to provide an accurate measurement of the polysilicon profile, particularly the top surface and edges thereof.

Because of the above-discussed differences between Claim 1 and the prior art, and because of the advantages associated with those differences, it cannot be said that Claim 1 is anticipated by or is obvious in view of the prior art. Claim 1, hence, patentably distinguishes over the prior art and is allowable. Claims 2-16 are dependent from Claim 1 and are allowable therewith.

In light of the above-discussion, the Examiner is asked to reconsider and to withdraw the rejection of Claims 1, 2 and 9 under 35 U.S.C. 102 and the rejections of Claims 3-8 and 10-16 under 35 U.S.C. 103, and to allow Claims 1-16. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully Submitted,

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